A Review on Analysis and Reusability of FPGA Implementation for I2C Protocol

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Abstract: I2C is a multi-master serial computer bus invented by Philips that is used to attach low-speed peripherals to a motherboard, embedded system, or cellphone. It is a two-wire, bidirectional serial bus that is Serial Data line (SDA) and Serial Clock line (SCL) which provides a simple, efficient method of data exchange between devices. This paper presents a method for implementation of I2C protocol for reusability. The method proposed the design divided into three levels. The levels are named as Protocol level, Signal level and Interface level. This concept is widely applicable for any high speed device or slow device. Reusability allows us to us a various master and slave pairs without any modification in the design. This design method is to be design in VHDL and implementation will be in the FPGA.

Key Words: *I2C protocol, FPGA, VHDL, SDA, SCL.*

I. Introduction

I²C (Inter-Integrated Circuit), pronounced *I-squared-C*, is a multi-master, multi-slave, single-ended, serial computer invented by Philips Semiconductor (now NXP Semiconductors). It is typically used for attaching lower-speed peripheral ICs to processors and microcontrollers. Alternatively I²C is spelled I2C (pronounced I-two-C) or IIC (pronounced I-I-C). I2C is a very popular serial data transfer protocol. The versatile I2C-bus is used in various control architectures such as System Management Bus (SMBus), Power Management Bus (PMBus), Intelligent Platform Management Interface (IPMI), Display Data Channel (DDC) and Advanced Telecom Computing Architecture (ATCA)[1]. The I2C system uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. The logic AND function is exercised on both lines with external pull-up resistors. Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL.

II. Theory Related Work

The I2C system uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. The logic AND function is exercised on both lines with external pull-up resistors.

START signal

A START signal, usually referred to as the S-bit, is defined as a high-to-low transition of SDA while SCL is high. The START signal denotes the beginning of a new data transfer.Fig.1 (a).

A *Repeated START* is a START signal without first generating a STOP signal. The master uses this method to communicate with another slave or the same slave in a different transfer direction (e.g. from writing to a device to reading from a device) without releasing the bus. Depending on the current status of the SCL line, a START or Repeated START is generated.

STOP signal

The master can terminate the communication by generating a STOP signal. A STOP signal, usually referred to as the P-bit, is defined as a low-to-high transition of SDA while SCL is at logical '1'.Fig.1 (b).

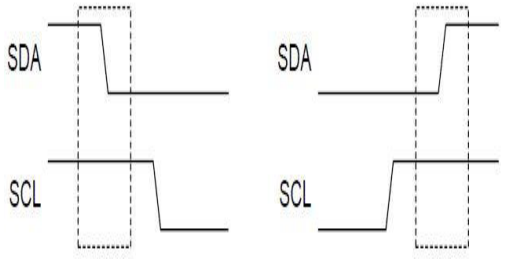

Fig. 1: (a) Start and (b) Stop Signal.

Transmitting a byte to a slave device

After start condition has been sent, a byte can be transmitted to a slave by the master. This first byte after a start condition will identify the slave on the bus (address) and will select the mode of operation. The meaning of all following bytes depends on the slave.

Receiving a byte from a slave device

Once the slave has been addressed and the slave has acknowledged this, a byte can be received from the slave if the R/W bit in the address was set to READ (set to '1').

Getting acknowledge (ACK) from a slave device

When an address or data byte has been transmitted onto the bus then this must be acknowledged by the slave(s). In case of an address, if the address matches its own then that slave and only that slave will respond to the address with an ACK. In case of a byte transmitted to an already addressed slave, the slave will respond with an ACK as well.

Giving acknowledge (ACK) from a slave device

Upon reception of a byte from a slave, the master must acknowledge this to the slave device. If there is no data left to receive, the master will send a not-acknowledge (NACK) signal and will stop the data transaction.

III. Literature Survey

The I2C bus was developed in the early 1980's by Philips Semiconductors. Its original purpose was to provide an easy way to connect a CPU to peripheral chips in a TV-set. Peripheral devices in embedded systems are often connected to the MCU as memory-mapped I/O devices, using the microcontroller's parallel address and data bus. This result in lots of wiring on the PCB's to route the address and data lines, not to mention a number of address decoders and glue logic to connect everything. In mass production items such as TV-sets, VCR's and audio equipment, this is not acceptable. In these appliances, every component that can be saved means increased profitability for the manufacturer and more affordable products for the end customer. Furthermore, lots of control lines implies that the system is more susceptible to disturbances by Electromagnetic Interference (EMI) and Electrostatic Discharge (ESD). The research done by Philips Labs in Eindhoven (The Netherlands) to overcome these problems resulted in a 2-wire communication bus called the I2C bus. I2C is an acronym for Inter-IC bus. Its name literally explains its purpose: to provide a communication link between Integrated Circuits. Today, the I2C bus is used in many other application fields than just audio and video equipment. The bus is generally accepted in the industry as a de-facto standard. The I2C bus has been adopted by several leading chip manufacturers like Xicor, ST Microelectronics, Infineon Technologies, Intel, Texas Instruments, Maxim, Atmel, Analog Devices and others[2].

Several competitors, such as Siemens AG (later Infineon Technologies AG, now Intel mobile communications), NEC, Texas Instruments, STMicroelectronics (formerly SGS-Thomson), Motorola (later Freescale), and Intersil have introduced compatible I2C products to the market since the mid-1990s.SMBus, defined by Intel in 1995, is a subset of I2C that defines the protocols more strictly. One purpose of SMBus is to promote robustness and interoperability. Accordingly, modern I2C systems incorporate policies and rules from SMBus, sometimes supporting both I2C and SMBus, requiring only minimal reconfiguration.Since October 10, 2006, no licensing fees are required to implement the I2C protocol. However, fees are still required to obtain I2C slave addresses allocated by NXP[3].*Zheng-wei HU, I2C Protocol Design for Reusability*: Third International Symposium on Information Processing –In this paper I2C protocol design method for reusability was proposed. In this method, design was divided into 3 levels: protocol level, signal level and interface level.The design method was design in VHDL, implemented in FPGA and applied in bio-logging design for RTC and light sensor which are based on I2C protocol. The data acquired by light sensor were transferred through RS232 to PC and stored into text file. The file was shown into graph by using Matlab. The data acquired by RTC were shown by RS232 tool[4].*Prof. Jai Karan Singh "Design and Implementation of I2C master controller on FPGA using VHDL,"* IJET, Aug-Sep 2012, the focus of this paper is on I2C protocol following master controller. This controller is connected to a microprocessor or computer and reads 8 bit instructions following I2C protocol. 32 bit register is designed to send data serially as per SPI instructions. The complete module is designed in VHDL and simulated in ModelSIM. This concept is widely applicable where a microprocessor wants to communicate with SPI device[5].*A.K. Oudjida, M.L. Berrandjia, R. Tiar, A. Liacha, K. Tahraoui "FPGA Implementation of I2C& SPI Protocols"* a Comparative Study IEEE 2009 I2C and SPI are the most commonly used serial protocols for both inter-chip and intra-chip low/medium bandwidth data-transfers.This paper contrasts and compares physical implementation aspects of the two protocols through a number of recent Xilinx's FPGA families, showing up which protocol features are responsible of substantial area overhead. This valuable information helps designers to make careful and tightly tailored architecture decisions. For a comprehensive comparative study, both protocols are implemented as general purpose IP solutions, incorporating all necessary features required by modern ASIC/SoC

applications according to a recent market investigation of an important number of commercial I2C and SPI devices. The RTL code is technology independent, inducing around 25% are overhead for I2C over SPI, and almost the same delays for both designs[6].*Arvind Sahu, Ravi Shankar Mishra, Puran Gour, Design and Interfacing of High speed model of FPGA using I2C protocol*: Int. J. Comp. Tech. Appl., Vol 2 (3), 531-536 ISSN:2229-6093. Sahu *et al.* developed inter IC protocol for data surveillance purpose. Data surveillance is very important application to monitor people or sensors.I2C is used for data surveillance because it could make system efficient, accurate, flexibility, and low development cost. They designed a protocol in VHDL and interface with OV7620 single chip CMOS VGA color digital camera. Data surveillance includes monitoring people or collection of sensors information from various nodes. They developed system which will replace traditional cameras with LAN cameras with complex image processing and IP routing. Data compression takes place with H.263 algorithm due to its high compression efficiency and high data rate. For surveillance constant bit rate limit the real time communication of cameras so variable bit rate is used. Variable bit rate efficiently uses available bandwidth.H.263 encoding is very complex normal DSP processor cannot handle it so FPGA as programmable solution is used. All results were verified using Modelsim and FPGA can be used as interface in between camera and local monitor system[7].*Madhuri Daware, Prof. A. S. Patil: IMPLEMENTATION OF I2C BUS PROTOCOL ON FPGA*, Dawaree*t. al* designed inter IC protocol using system VHDL and FPGA. Design mainly includes master design. Master design was implemented in Cyclone IV FPGA. I2C master is designed using VHDL by the of Finite State Machine. The low speed peripherals RTC (DS1302) and EEPROM are interfaced with I2C master bus through Nios-II Softcore Processor and implemented on Cyclone IV FPGA[8].*P. Venkateswaran, M. Mukherjee, A. Sanyal, R. Nandi ,"Design And Implementation Of FPGA Based Interface Model for Scale Free Network Using I2C Bus Protocol On Quartus II 6.0",International conference on computer and devices for communication and Devices for Communication* 2009. Researcher developed an interface model for scale free network using inter-IC bus protocol which includes master and slave design. Master was made up of different blocks as initiator, address block, write block, read block, clock generator. Initiator tested whether data bus was free to use or not. Address bit was transmitted by address block bit by bit to SDA line and after completion of address it reset SDA line to high position. Transmission and reception functions were performed by write and read block. All functions of master are governed by clock generator block. Slave was made up of design of monitor, address block, receiver and transmitter. Monitor function was same as initiator in master which sense the SCL and SDA line whether it is in use or not. Other blocks were functioned same as master block. Quartus II 6.0 was used to create VHDL model while it is simulated in Stratix II[9].

IV. Proposed Methodology

In our proposed design there are basically two parts of system. One is master and second is slave. The I2C system uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. The logic AND function is exercised on both lines with external pull-up resistors. Here, we will design the master part such that our system is capable for reuse. We will use the prebuild slave device for communication with master device.

Slave device may be an ADC, a DAC, Memory (RAM, SDRAM, Flash, EEROM, etc.), LCD or any other device. Here we may use memory device for implementation as a slave.

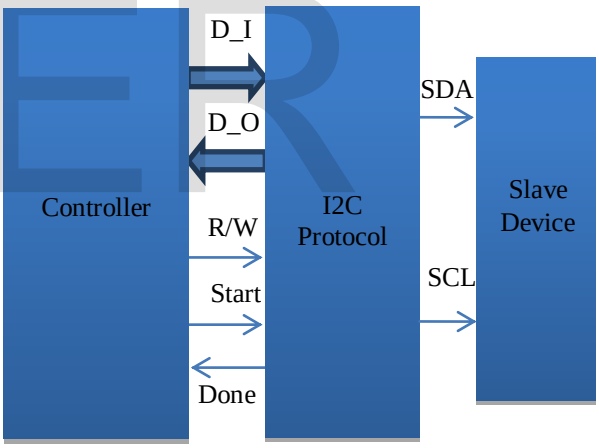

Fig. 2: Proposed Block Diagram

Above fig. shows the basic concept of I2C protocol communication. The controller issues the read or write command and accordingly the I2C protocol perform the operation. In our design we will make input lines open ended so that any device can be connected to the I2C bus as a master device, unlike in I2C compatible devices where I2C protocol is inbuilt in IC package. The problem with design of system using I2C communication is the compatibility of devices used in system, with the I2C protocol. In such system when we want to change the device, new device must be I2C compatible. To solve this problem we have define this method.

Design Requirements:

To design the I2C protocol for reusability we need to design a code and then burn it into hardware so the design can be checked physically and output is directly visible. Therefore in designing the protocol we require the simulation software to simulate and the design code, synthesis software and hardware. So, we will use the Active-HDL for simulation and FPGA of Altera. The coding will in the VHDL. And make the use of Finite State Machine to design the protocol.

V. Conclusion

The ideal I2C bus has high performance, flexibility and low cost. The proposed method will be design in VHDL and we will create the model in FPGA, so it will allow rapid prototyping of the interface model for large scale communication. We will try to design and simulate the proposed methodology.

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